

SILICON-ON-INSULATOR CHIP HAVING AN ISOLATION BARRIER FOR RELIABILITY

ABSTRACT

An SOI chip having an isolation barrier. The SOI chip includes a substrate, an oxide layer deposited on the substrate, and a silicon layer deposited on the oxide layer. A gate is deposited above the silicon layer. A first metal contact is deposited above the gate to form an electrical contact with the gate. Second and third metal contacts are deposited to form electrical contacts with the silicon layer. The isolation barrier extends through the silicon layer and the oxide layer, and partially into the substrate, to block impurities in the oxide layer outside the isolation barrier from diffusing into the oxide layer inside the isolation barrier. The isolation barrier surrounds the gate, the first metal contact, the second metal contact, and the third metal contact--which define an active chip area inside the isolation barrier. A method of manufacturing the SOI chip is also disclosed.